REMARKS

In the Final Office Action dated February 24, 2004, the Examiner has *finally rejected* claims 8, 9, 14-17, and 19-22 pending in the present application. Reconsideration and allowance of pending claims 8, 9, 14-17, and 19-22 in view of the following remarks is respectfully requested.

A. Rejection of Claims 8, 9, 17 and 22 under 35 U.S.C. § 102(e)

The Examiner has rejected claims 8, 9, 17, and 22 under 35 USC §102(e), as being anticipated by U.S. Patent Application Number 6,429,072 B1 to ("Tsukiji"). For the reasons discussed below, Applicant respectfully submits that the present invention, as defined by independent claims 8 and 9, is patentably distinguishable over Tsukiji. However, Applicant reserves the right to provide declarations and/or documents under 37 CFR §1.131 to "swear behind" the effective filing date of Tsukiji.

As discussed in the present application, there has been a need in the art for a NAND memory device having improved reliability. Specifically, there has been a need in the art for a NAND array that has an improved silicon-tunnel oxide interface that reduces the potential for breakdown or current leakage in the overlap region while maintaining a relatively high injection field for programming and erasing functions.

As further highlighted in the present application, a high risk area for oxide breakdown or current leakage exists in the oxide layer, source/drain overlap region. In embodiments according to the present invention, a NAND-type memory cell has a tunnel

oxide layer formed over the active region of the substrate such that the thickness of the tunnel oxide in the overlap region is greater than the thickness of the tunnel oxide in the channel region.

For a given voltage, an increase in the thickness of the tunnel oxide layer portion in the overlap region causes the injection field at the overlap region to be reduced. By reducing the injection field in the overlap region, the potential for oxide breakdown and/or current leakage in the overlap region is reduced as well. The tunnel oxide layer portion overlaying the channel region of the active region is thinner than the oxide layer in the overlap region, thus ensuring that a suitable injection field is attained for programming and erasing functions.

Various advantages of the present invention are a result of the invention as disclosed and claimed in independent claims 8 and 9. For example, independent claims 8 and 9 recite "a gate insulating layer situated over an entire length of said third region and substantially less than an entire length of each of said first region and said second region." (Emphasis added.)

The cited art, Tsukiji, discloses a floating gate memory cell structure. Nevertheless, upon review of, for example, Figures 5E, 5F, 5G, and column 6, lines 44-47 of Tsukiji it is readily apparent that "insulation films 122 extend on inside walls and top surfaces of the source side and drain side interconnections 104a and 105a." This configuration is in stark contrast to the "substantially less" language of novel independent claims 8 and 9 of the present application.

In fact, Tsukiji teaches away from the invention of claims 8 and 9, wherein the configuration of the gate insulating layer advantageously reduces the potential for oxide breakdown and/or current leakage in the first and second regions (i.e. the source and drain regions). Tsukiji teaches insulation films 122 that extend the entire top surfaces of the source side and drain side interconnections 104a and 105a. (See Figures 5E, 5F, 5G, and column 6, lines 44-47.)

Consequently, the potential for oxide breakdown and current leakage in the source and drain regions of Tsukiji increases, due to, for example, the capacitance created by the overlap of insulation films 122 on the interconnections 104a and 105a, which run the entire length of drain and source regions 104 and 105. Moreover, because the insulation films 122 run the entire length of the drain and source regions 104 and 105 (with conductive interconnections 104a and 105a therebetween), more oxide breakdown and current leakage will occur in the drain and source regions 104 and 105 of Tsukiji.

Accordingly, it is respectfully submitted that independent claims 8 and 9 and their respective dependent claims 17 and 22 are patentably distinguishable over Tsukiji and should be allowed.

B. **Rejection of Claims 14-16 and 19-21 under 35 U.S.C. § 103(a)**

The Examiner has rejected claims 14-16 and 19-21 under 35 U.S.C. §103(a), as being unpatentable over Tsukiji in view of U.S. Patent Number 6.432,762 to Libera et al. ("Libera"). Applicant respectfully submits that claims 14-16 depend from claim 8 and

claims 19-21 depend from claim 9, and thus, claims 14-16 and 19-21 should be allowed at least for the same reasons discussed above in conjunction with patentability of claims 8 and 9.

C. **Conclusion**

Based on the foregoing reasons, the present invention, as defined by independent claims 8 and 9, and claims depending therefrom, is patentably distinguishable over the art cited by the Examiner. Thus, claims 8, 9, 14-17, and 19-22 pending in the present application are patentably distinguishable over the art cited by the Examiner. As such, and for all the foregoing reasons, an early Notice of Allowance of claims 8, 9, 14-17, and 19-22 pending in the present application is respectively requested.

Attorney Docket No.: 0180129

Respectfully Submitted,
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Date: 4/26/04

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